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DEC 76 J E BREWER, T G O'DONNELL, P C SMITH DAAB07-76-C-0048

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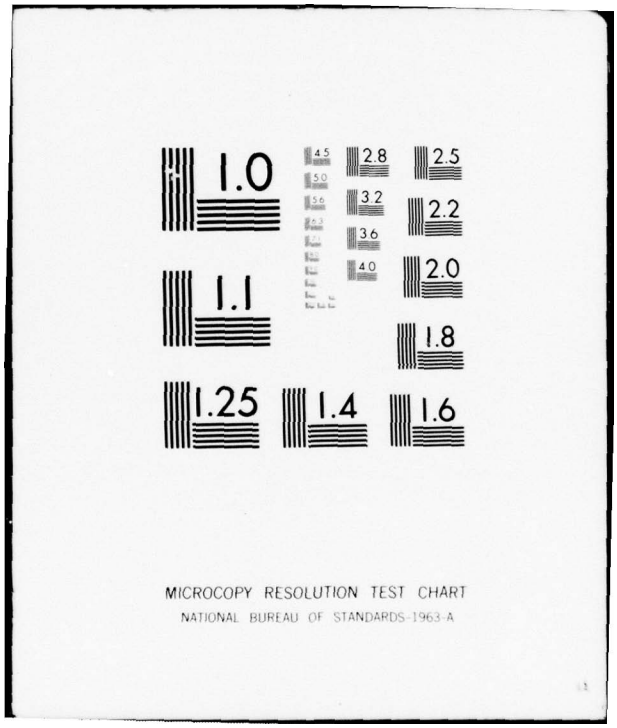
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MNOS BORAM MANUFACTURING METHODS AND TECHNOLOGY PROJECT

Second Quarterly Progress Report
1 October 1976 to 31 December 1976

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TECHNICAL REPORT

MNOS BORAM MANUFACTURING METHODS AND TECHNOLOGY PROJECT

Second Quarterly Progress Report

1 October 1976 to 31 December 1976

Prepared by

J.E. Brewer, T.G. O'Donnell, P.C. Smith, L.A. Epstein

PROJECT OBJECTIVE: Establish a production capability for metal nitride oxide semiconductor (MNOS) integrated circuits for block oriented random access memory (BORAM).

Contract DAAB07-76-C-0048

WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER
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ABSTRACT

A manufacturing methods project has been initiated to establish a pilot production line for metal nitride oxide semiconductors (MNOS) block oriented random access memory (BORAM) multichip hydrid circuits. During the past quarter the hybrid circuit configuration was finalized, electrical test procedures were defined, and a new low cost MNOS die was fabricated. In addition process studies were continued, and the results of Auger analysis were summarized.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

PURPOSE

The purpose of manufacturing methods and technology (MM&T) project number 2769758 is to establish a production capability for metal nitride-oxide semiconductor (MNOS) integrated circuits for block-oriented random access memory (BORAM).

Military organizations are faced with a difficult hardware problem in the use of modern day computers. A suitable militarized secondary storage technology simply does not exist. Drums and discs cannot stand up under the stress of the ground mobile environment. Military real time programs are forced to be resident in main memory because electromechanical storage access delays cannot be tolerated.

MNOS BORAM holds considerable promise of meeting the military's secondary storage needs. An advanced development Army/Navy MNOS BORAM module has proven that significant volume, weight, power and use flexibility advantages can be achieved. When compared to fixed-head electromechanical storage MNOS BORAM offers MTBF's 10 times longer, and access times about 500 times faster.

This MM&T project will establish for the government a source of supply for MNOS BORAM secondary storage. A pilot production line with a demonstrated capacity of 1,875 hybrid circuit per month will be established. Each hybrid circuit will contain 16 MNOS BORAM integrated circuits. This production rate will provide sufficient hybrid circuits to allow fabrication of three 16.8 megabit BORAM modules per month. The hybrid circuits will conform to Electronics Command Technical Requirement SCS503, and the MM&T project will be conducted in accord with Electronics Command Industrial Preparedness Procurement Requirement Number 15.

1. NARRATIVE AND DATA

Preparations for establishment of an MNOS BORAM pilot line are proceeding smoothly. The final version of the hybrid circuit has been established. Test strategies and test programs are maturing. Die size reduction appears successful. Equipment for timely evaluation of transistor characteristics has become available. Analysis of the nitride and tunneling layer is continuing. The production line has continued to operate at a low level to support experimentation and process tuning.

1.1 MULTICHIP HYBRID MICROCIRCUIT

Design of the multichip hybrid circuit has been finalized. Substrate layout is complete. Package requirements have been defined and procurement is underway.

1.1.1 Circuit Description

Figures 1-1 and 1-2 document the circuit connections for the BORAM memory microcircuit. The circuit contains 16 of the MNOS BORAM 6002 chips. Except for data and chip select lines the chips are simply connected in parallel.

Power dissipation per hybrid will be very low. Normally all chips are powered down. When a data transaction is required, power will be applied to the microcircuit. At that time one of the chip select lines (one of eight) will be enabled. The two chips associated with that line will then become active. The total package dissipation during this active period will rise to roughly, 400 milliwatts. Immediately after the data transaction the chip select will be disabled, and the power removed. Junction temperatures on active chips should remain within 3°C of the case temperature.

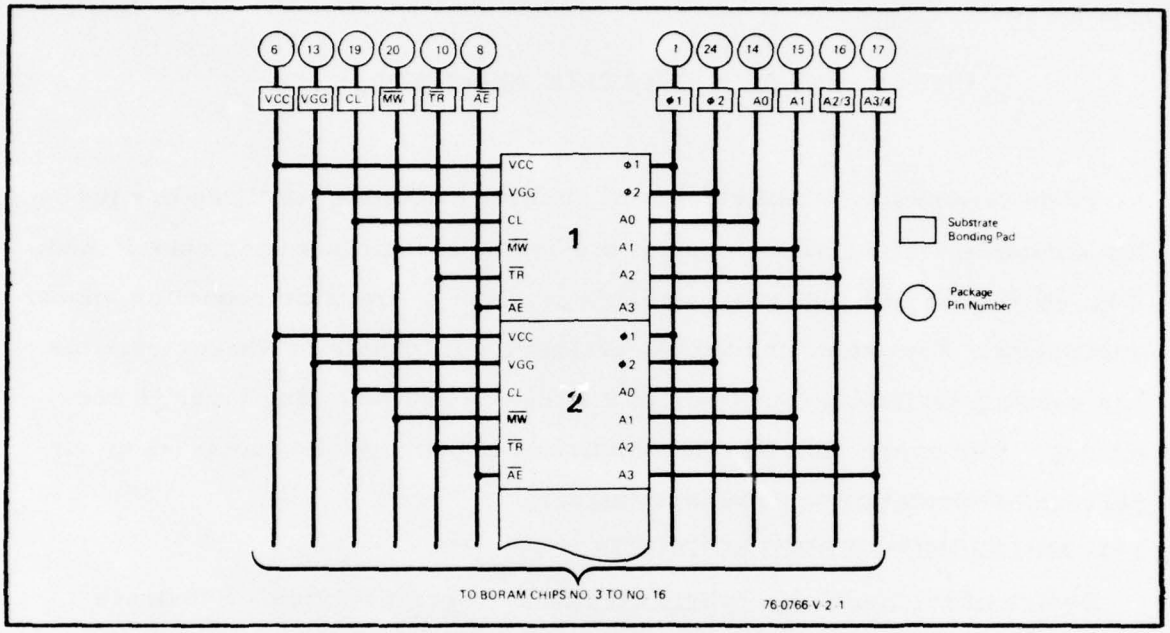

Figure 1-1. Bussed Connections in BORAM Memory Microcircuit

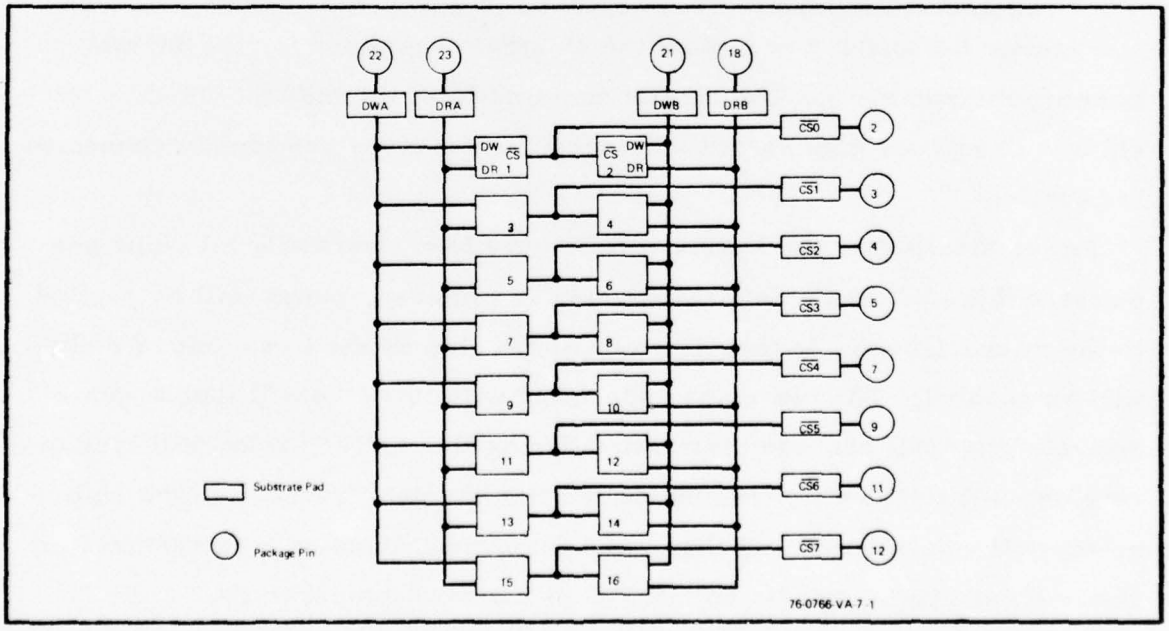

Figure 1-2. BORAM Memory Microcircuit Data I/O and Chip Select Connections

The microcircuit has two data inputs (DWA and DWB) and two data outputs (DRA and DRB). The "A" data lines are associated with the eight odd numbered chips. The "B" data lines are associated with the eight even numbered chips. Each chip select line controls one odd and one even numbered device. Data outputs are tristate. A deselected chip is in a high impedance state. A selected chip controls the output bus, and has both active sink and source capability.

1.1.2 Substrate Design

A multilayer alumina substrate is used to interconnect the MNOS BORAM chips. Substrate layout has been planned to allow manufacture by multiple sources using different fabrication approaches. Dimensions have been established to allow tape carrier bonding or wire bonding. Provisions have been made to facilitate fault isolation in the event of chip failure.

The substrate dimensions are 1.700 by 0.780 by 0.050 inches. Interconnection is accomplished by four metal layers. Layers are separated and supported by a dielectric material. Layer to layer connections are made by 0.015 by 0.015 inch vias.

The top metal layer is exposed, and provides pads for wire bonding. Chip to substrate and substrate to package lead connections are made to this layer. The chips may alternatively be mounted on the substrate using tape carrier technology. Figure 1-3 shows an assembled hybrid. The bonding pad locations with respect to the chips are visible.

1.1.3 Package Description

A package procurement specification has been developed, and the procurement process is underway. The package has been defined to be compatible for use as a short term learning vehicle, and for evolution toward a long term optimum cost-reliability tradeoff.

Package external dimensions are 1.036 by 1.925 inches. The case is 0.135-inch high. Pins are positioned on 0.1-inch centers. As shown in figure 1-3, pin number 1 and pin number 24 are 0.2 inch away from the

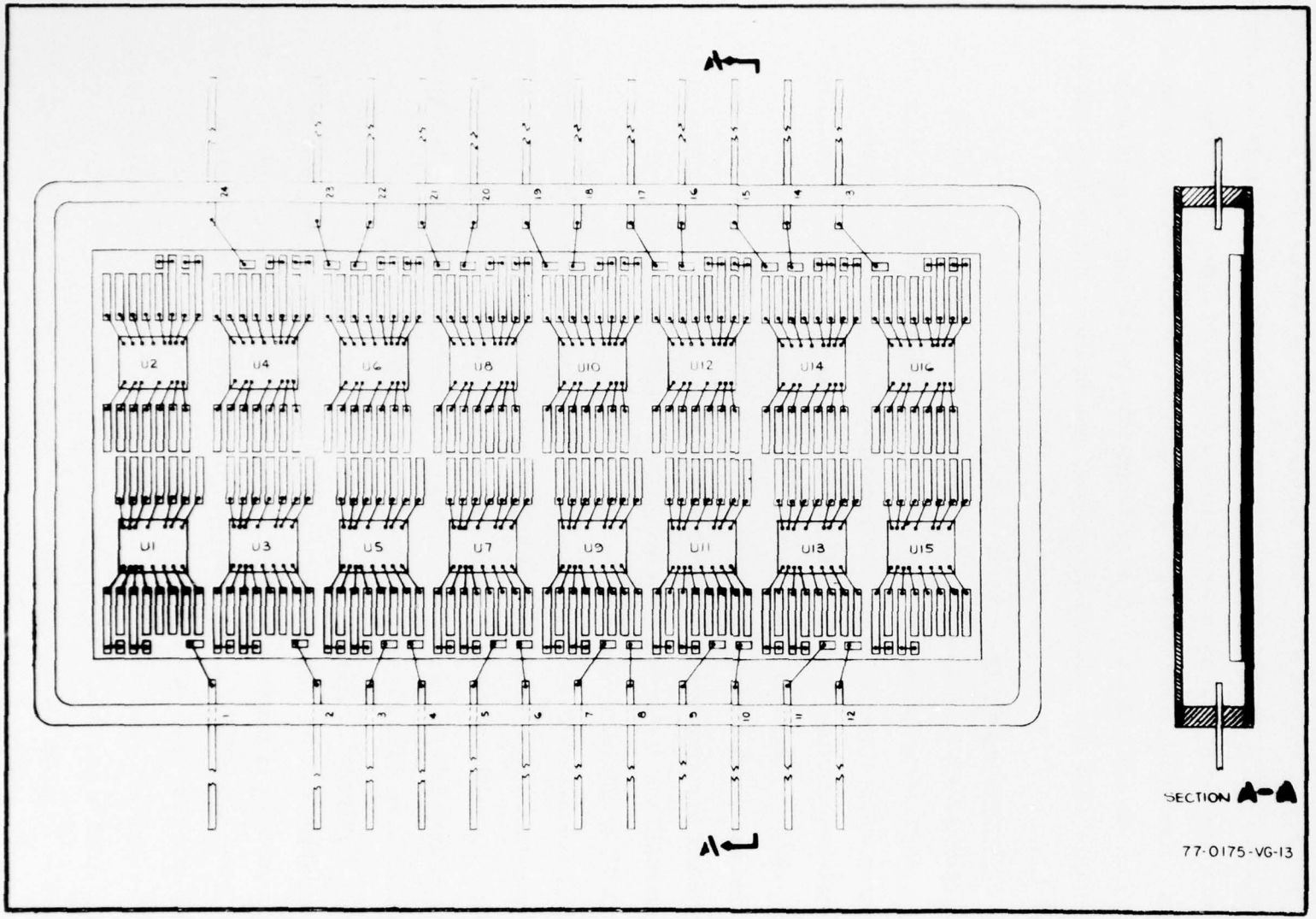

Figure 1-3. BORAM Memory Microcircuit

adjacent pin. This makes it impossible to insert the package into the printed circuit board improperly. The leads and dimensions are compatible with existing production line tooling.

Initially the package will be procured with gold plating and the lid will be solder sealed. This allows the use of existing processes and tooling. Later, the option of nickel plating and a welded lid will be explored. The elimination of gold will reduce costs. The use of a welded lid will improve reliability and allow repair (i.e., the lid may be removed and resealed).

1.2 BORAM 6000C ELECTRICAL TEST

After wafer processing, electrical probe testing is performed to determine which die are functional. It is a characteristic of BORAM chips that a very thorough test can be performed at this stage. Probe capacitance and the thermal environment do not distort the test results. An important part of this MM&T project is to address the unique test requirements for MNOS devices, and to establish automatic test programs suitable for use in volume production.

1.2.1 Test Strategy

The considerations associated with a production probe test are relatively straight forward. The test sequence should be designed to achieve minimum test time- i.e., minimum test cost. Reject die should be eliminated as quickly as possible. On the other hand, good die must be thoroughly tested to avoid costs of replacement after packaging. The screen must treat the unique MNOS test problem of identifying die with possible retention and/or endurance marginality. Finally, the program should gather data for statistical production control purposes.

Figure 1-4 shows the outline plan for BORAM testing. Seven categories of tests will exist in the final version of a probe test. This same structure will be used for testing individual packaged chips and multichip hybrid circuits.

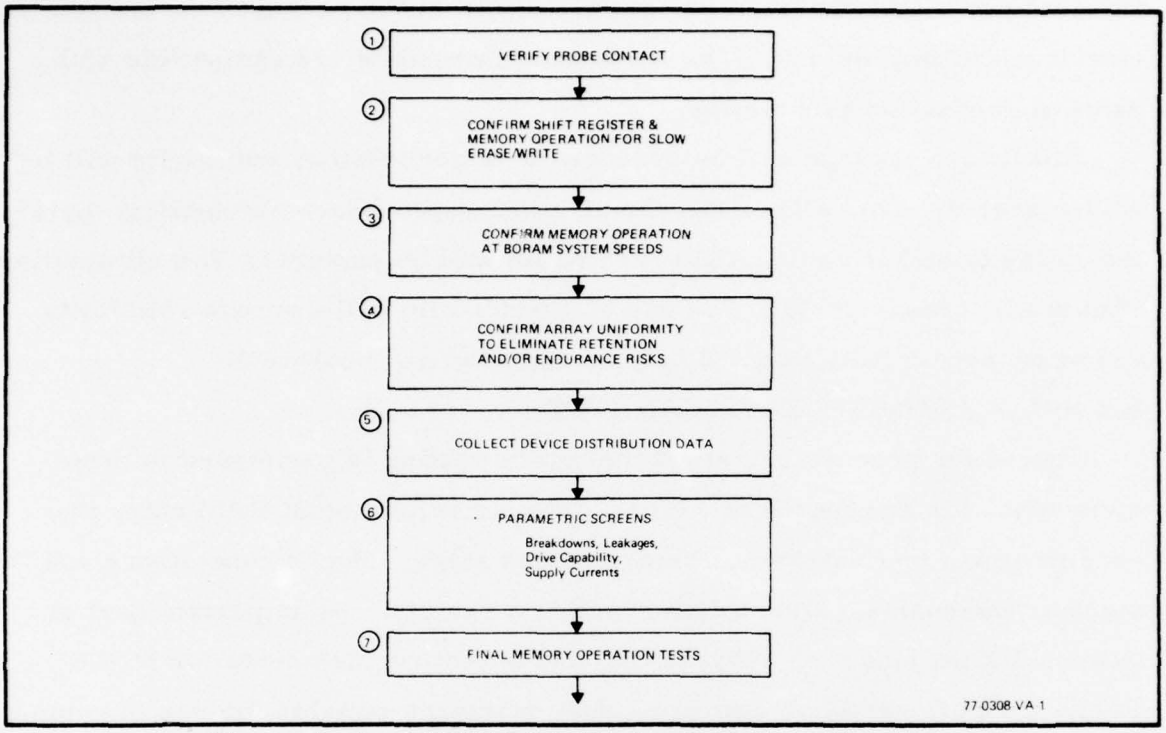

Figure 1-4. MNOS BORAM Logical Test Sequence

The initial test category consists of checking the forward voltage of the substrate diode associated with every input pad. The primary purpose of the test is to give the machine operator immediate feedback as to whether a probe contact problem exists. The test also will detect aluminum to silicon contact or gross junction problems.

The second test category has the objective of rejecting nonfunctional die immediately. These functional tests proceed at high speed, and will expend a minimum amount of time on problem die. The scheme is to exercise the shift register using simple data patterns; then erase, write and read the memory at slow speed. The data pattern written into memory should place unique data in each word so that proper addressing is verified.

Die which pass category 2 tests provide a measure of the quality of the wafer processing. The shift register yield and the entire array yield can be related to the respective die areas to compute an effective defect density.

Category 3 tests exercise the memory chip at nominal BORAM system operating conditions. Data patterns different from those of the category 2 tests should be used. This screen eliminates parts with gross pulse response problems or control and detection circuit dynamic problems.

In category 4 tests, the screening process is extended to examine parts for nonuniformity or marginality. The emphasis is on identification of parts that are high risk from the viewpoint of long term data retention and/or possible overstress with accumulated erase write cycles. These tests also examine dynamic performance margins internal to the device.

Category 5 tests exist to allow product engineers to monitor and learn about the statistical distribution of key product characteristics. The automatic test equipment does not accept or reject parts on the basis of these tests. Test results are recorded for each die, and are subjected to various data reduction procedures.

The category 6 parameter tests involve relay switching, and therefore, require more machine time than functional tests. By performing these tests only on parts that have been found to be functional considerable test time is saved. This test battery examines all terminals for proper dc characteristics. Breakdown voltages, leakage currents, source and sink capability, and supply currents are exhaustively checked.

As a final confirmation of performance, and a check that no device failure occurred during testing, the memory operation is again checked at nominal system operating conditions. The category 7 test is a repeat of the category 3 test.

1.2.2 Test Description and Results

Figure 1-4 serves as a model of the desired wafer probe test for the 6000C chip. Full implementation, however, requires a detail knowledge of the product characteristics and statistical distribution. Therefore, it is necessary to approach the "final" program through a series of programs designed to gather the necessary information.

Figure 1-5 describes the present version of the wafer screen. The most notable descrepancy from the test model is the absence of any category 4 tests. At this stage of development, extensive category 5 characterization tests are being performed to lay the ground work for eventual incorporation of the category 4 screens.

Four aspects of device performance are being explored. The array is tested using write pulses that vary from 1 microsecond to 100 microseconds to establish the minimum usable write pulse. A binary search algorithm is employed to quickly converge on the minimum. Array nonuniformities and/or retention defects are expected to be easier to detect in parts that are marginally written.

It has been noted that arrays which exhibit poor retention sometimes exhibit voltage sensitivity when written with short write pulses. To explore the possibility of using this property for screening, each chip is being characterized for VDD voltage operating range when written with a 10-microsecond pulse. Voltages from -12 to -22 volts are searched using a binary algorithm.

A third characteristic of interest is the substrate voltage level during erase. The voltage level can be affected by isolation junction leakage currents. Devices with gross leakage will not erase properly, and will be eliminated by category 2 and 3 tests. The devices that survive to be characterized will include some population of border line chips. Tabulations of the erase voltage levels will quantify the magnitude of the problem, and will allow establishment of intelligent parametric test limits.

Finally, a battery of tests are performed on the test structures included on each 6000C chip. The pulse response of the memory transistor is explored using various erase, write and read combinations. The threshold voltage is recorded after each test.

The other tests indicated in figure 1-5 can be understood directly from the diagram. The notation B20, B19 to B0 refers to the "bin" numbers

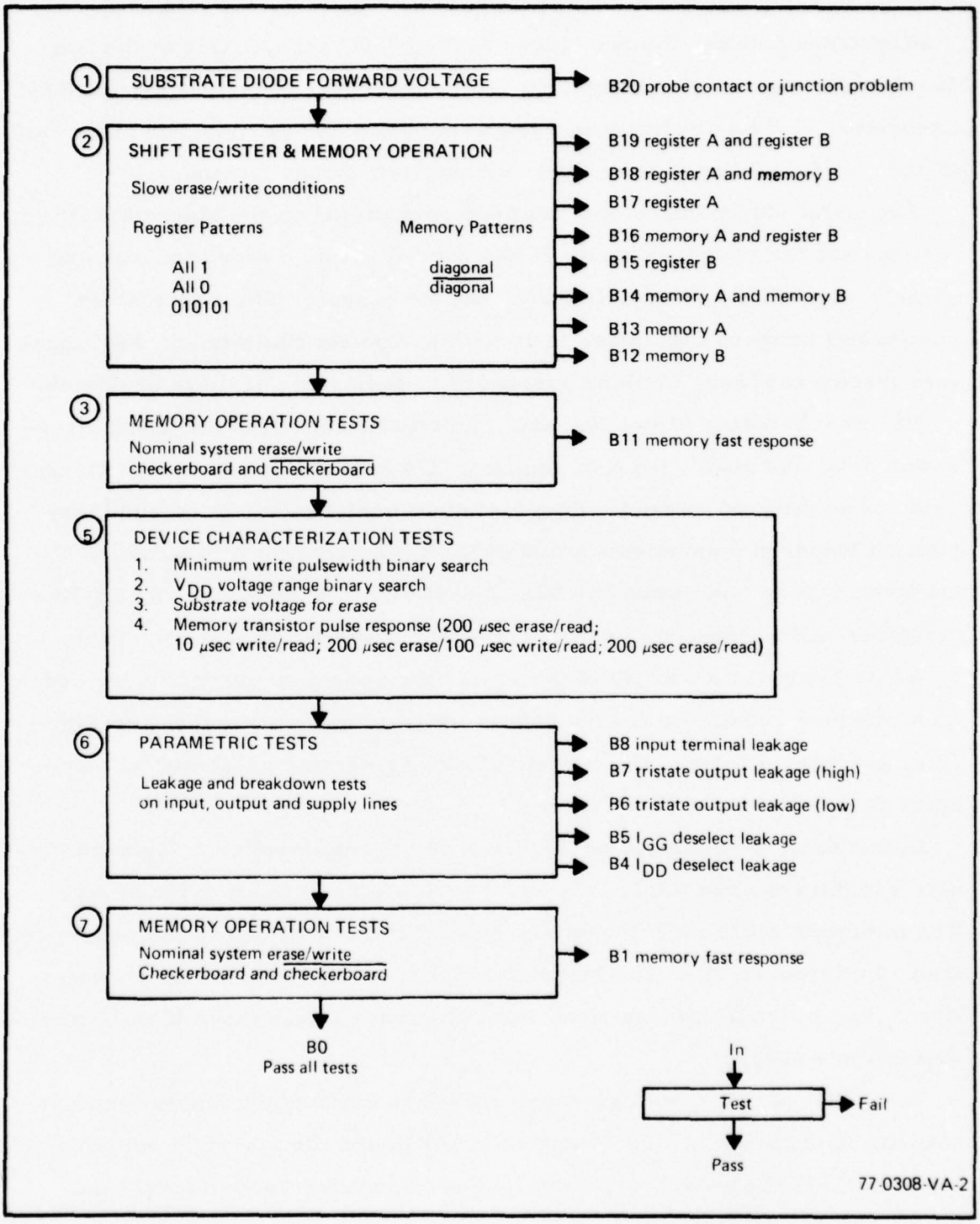

Figure 1-5. BORAM 6000C Wafer Probe Test Flow Diagram

used by the Macrodata 154 test system. In category 2, the test program distinguishes between the two halves of the 6000C array. One of the two 16-bit shift registers is designated as "register A". The 1024 bits of RAM associated with that register is designated as "memory A". The other half of the chip is similarly referred to a "register B" and "memory B".

The 6000C wafer probe test has been operational on the Macrodata 154 test system for sometime now. It has proved to be an excellent learning vehicle as well as an adequate functional die screen. The major short comings of the probe test have to do with equipment limitations. Additional test system hardware is being purchased to ease some of these problems.

Efficient handling of the test data (both test summaries and characterization data) has been a point of concern. On-line printout from the Macrodata 154 is difficult to read. Preparation of useful information summary reports required manual data transcription. To correct this situation a magnetic tape output option has been purchased. In the future, an off-line computer will prepare test reports from the magnetic tape source data.

Table 1-1 gives a sample of the variables types data currently derived from the probe test. Variables data is obtained from parts that survive to enter category 4 tests. The results of other tests are presented as attributes data in the form of bin counts.

Information is presented on 15 die from a single wafer. This particular sample required fairly long write pulsewidths to operate the array. The minimum write search routine shows that many devices required more than 10 microseconds. The last die exhibited a very long minimum write time. For current process conditions, die that require more than 20 microseconds are suspect.

The VDD operating voltage range search is conducted using two complementary data patterns. The Macrodata 154 prints the last trial voltage attempted. If the search could not find any operating voltage level, the letter "F" follows the voltage value.

TABLE 1-1

SAMPLE 6000C WAFER PROBE TEST RESULTS

Die Ref No.	Minimum Write Pulsewidth Search	V_{DD} Voltage Search Most Positive Voltage		Erase Substrate Voltage	Memory Transistor Pulse Response			Lowest Input Breakdown Voltage
		Checkerboard	$\overline{\text{Checkerboard}}$		V_{HC} for 200 μsec Erase	V_{LC} for 10 μsec Write	V_{LC} for 100 μsec Write	
	(Microseconds)	(Volts)	(Volts)	(Volts)	(Volts)	(Volts)	(Volts)	(Volts)
1	13.6	−22.0F	−15.8	−26.2	2.9	9.1	10.8	>40
2	8.5	−12.0	−12.0	−26.2	3.0	9.3	10.9	>40
3	11.2	−12.0	−12.0	−25.4	3.3	9.1	10.8	>40
4	12.2	−18.8	−18.6	−26.1	2.9	9.2	10.9	>40
5	13.8	−12.0	−12.0	−22.3	4.3	9.0	10.8	>40
6	10.5	−12.0	−12.0	−24.1	3.6	9.2	10.9	33
7	4.2	−12.1F	−12.0	−24.1	3.0	9.4	11.0	>40
8	12.8	−12.1F	−12.0	−26.0	3.0	9.4	11.0	>40
9	7.5	−12.0	−12.0	−26.1	3.4	9.6	11.4	>40
10	7.9	−12.1F	−12.0	−26.1	3.0	9.6	11.3	>40
11	18.2	−22.0F	−22.0F	−22.5	5.1	9.0	10.9	>40
12	18.6	−22.0F	−22.0F	−22.5	5.4	9.1	10.9	>40
13	7.7	−12.0	−12.0	−25.6	3.4	9.6	11.4	>40
14	9.6	−12.0	−12.0	−25.7	3.9	9.5	11.3	>40
15	75.6	−22.0F	−22.0F	−25.7	4.3	9.4	11.3	>40

*Data taken on wafer 3 from lot 4502A.

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The VDD test results illustrate some of the learning aspects of the probe tests. The search is performed using a 10-microsecond write pulse. It would be expected that parts which show a minimum write pulsewidth greater than 10 microseconds would have either a limited VDD range or no VDD range. For the most part this is true, but some inconsistances exist in the data. Part 3 for example passed the VDD search for the full -12 to -22 volts, but had an 11.2-microsecond minimum write pulsewidth. As the effort proceeds these discrepancies will be further investigated.

The substrate voltage during erase is the voltage applied across the gate structure of array memory transistors. It is a critical parameter for both pulse response and endurance. In the 6000C, the voltage level is established by the VGG supply, nonmemory transistor threshold voltage, body effect, and possible isolation junction leakage current. For this test sample, the voltage varied from -22.3 to -26.2 volts. Improved control over this voltage is desirable, and the new 6002 chip design did address this matter.

The next three columns in table 1-1 shows data obtained from a memory transistor test structure located on the 6000C die. This pulse response information is suitable for identification of gross problems. The VT tester is used to obtain a more complete picture of transistor performance.

The final column is obtained from the category 6 parametric tests. As the input terminal breakdown voltages are checked, the last voltage tested is saved. The test terminates on a failure (i.e., < 40 volts at 5 microamperes), and the voltage is printed.

In further test program development emphasis will be given to the 6002 chip. Data derived from the 6000C and from the VT tester will help to formulate test conditions and limits.

1.3 BORAM 6002 STATUS

The BORAM 6002 chip is the result of efforts to shrink or simplify the older 6000C device. At the close of the quarter the first 6002 material was fabricated. These comments review the nature of the new integrated circuit, and describe the results achieved with the first lot.

1.3.1 Design Goals

Prior to initiating the 6002 design a study was performed to establish design goals. Both system level and component level factors were considered. The many successful features of the 6000C circuit were to be preserved. No high risk innovations were to be introduced.

The general objectives were to reduce die area, reduce the pin count, minimize the number of high level signals, and minimize the magnitude and number of supply voltages.

From a chip yield viewpoint, it was desired to reduce the amount of circuitry included in isolation tubs. Isolation junction leakage during erase can cause an objectional variation in the erase voltage amplitude. Less isolation junction area should lower the probability of encountering this problem.

From a system complexity viewpoint, it was found to be advantageous to reduce the amount of off-chip peripherial circuitry required on a memory card. Two approaches were readily apparent. The number of address drivers could be reduced by using on-chip address multiplexing. The number of data buffers could be cut in half by going to one shift register instead of the two used in the 6000C.

Future system growth was also a point of some concern. The rapid pace of integrated circuit technology has in the past generated some problems for the systems manufacturer. In order to be competitive, he designs using the best IC available. Within 6 months or a year that device is obsolete. How can he protect his investment in card layouts, test programs, documentation, production tooling, etc?

The 6002 design was constrained to have a pin-out that would be compatible with future chip designs. For example, an 8,192-bit chip can be provided at a later date as a pin for pin replacement of the 6002. Hybrid circuits and memory cards established for the 6002 should be usable for a larger device without change. System modifications to use a larger chip would be minimal.

1.3.2 Circuit Description

The BORAM 6002 integrated circuit is a nonvolatile block-oriented read/write memory device designed for use in computer secondary storage systems. Because of wide circuit design margins and a small die size, the 6002 provides a major cost improvement over previous BORAM devices. Figure 1-6 is a photograph of the 6002 die.

Within the 6002, information is stored in metal-nitride-oxide-semiconductor (MNOS) memory transistors by trapping charge at the nitride-oxide interface in the dual dielectric gate insulator. Charge may be inserted or removed electrically. Power supply and signal voltages may be removed from the chip and the charge will remain intact for long periods of time. After being written with a 100-microsecond pulse, the 6002 is required to retain data for 4,000 hours independent of the presence or absence of power supply voltages.

Individual memory cells consist of two drain-source protected (DSP) memory transistors. Differential circuits are used in the 6002 to reduce sensitivity to manufacturing process variation, supply levels and temperature changes. The detection circuitry can reliably distinguish threshold voltage differences as small as 0.1 volts, and is immune to any disturbing factors which affect both transistors in a cell. No external read reference voltages are required. The operating temperature range is -55°C to +125°C.

As shown in figure 1-7, the 6002 has 15 pins. All signals swing a nominal 0 to -15 volts except chip select ($\overline{CS}$) which swings 0 to -35 volts. Signals are referenced to V_{cc} which is taken as 0 volts. The V_{gg} supply is nominally -30 volts. Power dissipation when operating is less than 200 mW. The address inputs are multiplexed and latched internally to save address pins. The data output line DR is tristate, and will enter the high impedance state if chip select ($\overline{CS}$) is high.

The chip incorporates many features to ensure reliability and to avoid problems during assembly. Bonding pads are greater than 5 $mils^2$, and

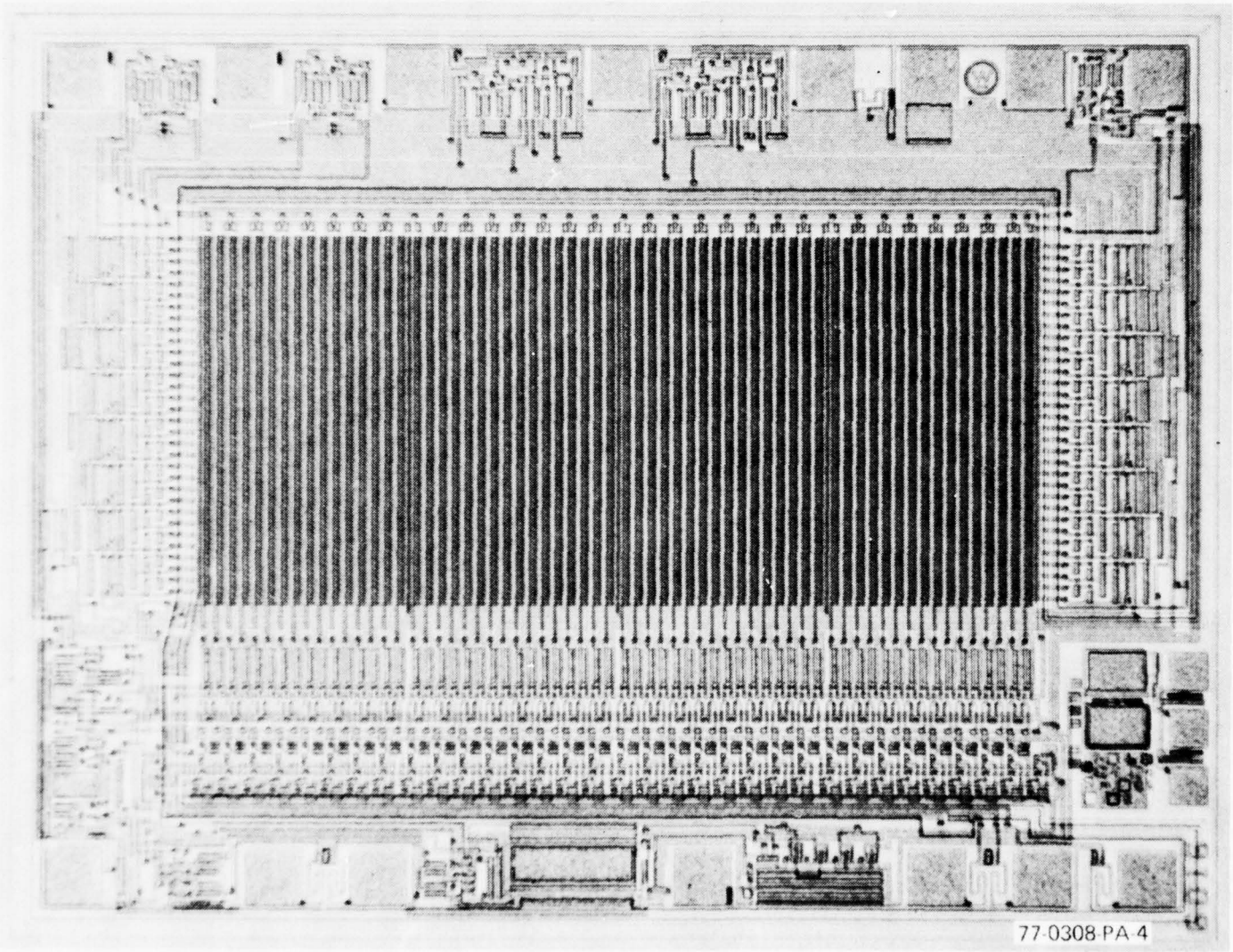

Figure 1-6. BORAM 6002 Die

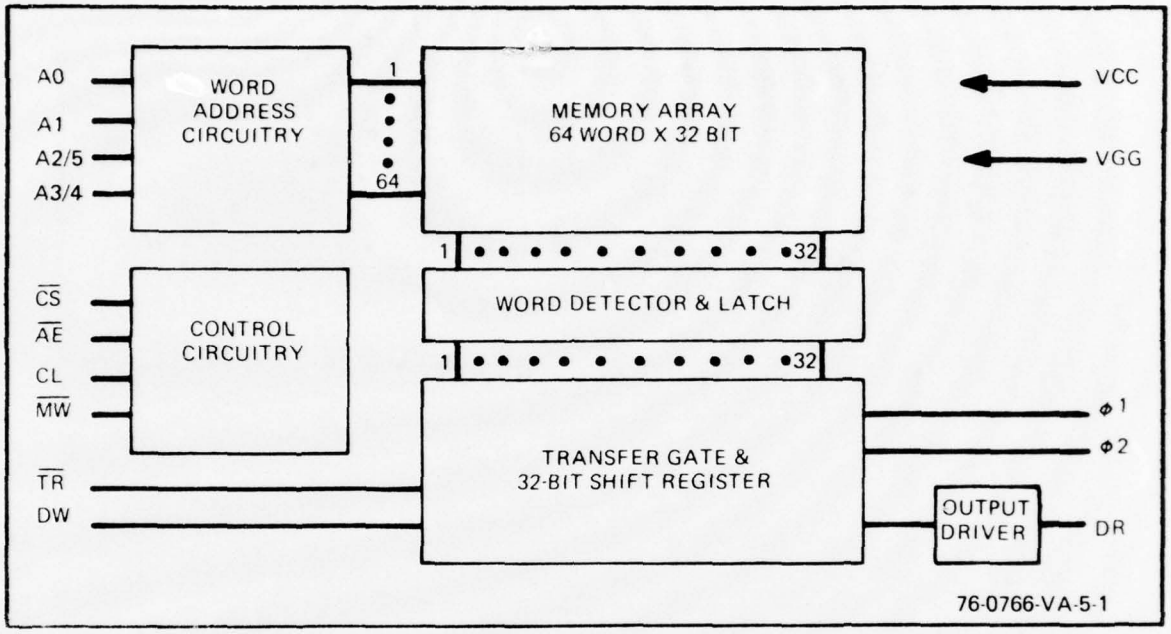

Figure 1-7. BORAM 6002 Functional Block Diagram

are positioned on opposite sides of the die to allow efficient use of space in the hybrid circuit. The nitride layer in the gate dielectric serves as an ion migration barrier and eliminates reliability failures because of latent oxide defects. A glass overcoat guards against scratches due to handling. Protective devices on all inputs avoid damage by static charge.

The 6002 die measures 2.5 x 3.3 mm^2 (99 x 128 $mils^2$), and features a 1020-μm^2 (1.58 mil^2) two-transistor cell. The ratio of array area to die area is 0.26. When judged in the context of contemporary MNOS die as shown in table 1-2, the 6002 layout is seen to be rather efficient. The two-transistor cell in the 6002 is almost one-half the size of the 6000C cell. In fact, it approaches the dimensions of some of the one-transistor cells. Only the Westinghouse 7006 chip which uses a polysilicon gate in the array region has a significantly higher density.

TABLE 1-2

EXAMPLES OF CONTEMPORARY MNOS DIE

IDENTIFICATION	DESCRIPTION	DIE SIZE (mils x mils)	CELL SIZE (mil^2)	ARRAY TO DIE AREA RATIO
Ⓦ 6000C	2 k, 2 FET cell	163 x 169	2.95	0.22
Ⓦ 7006	16 k, 1 FET cell	135 x 200	0.49	0.30
NCR 1105	1 k, 2 FET cell	147 x 115	2.80	0.17
NCR 2401	4 k, 1-1/16 FET cell	160 x 164	1.40	0.22
NCR 2800	8 k, 1-1/16 FET cell	197 x 227	1.40	0.26
NCR 3400	4 k, 1 FET cell	240 x 187	1.60	0.15
NCM 7040	256 bits, 2 FET cell	125 x 125	2.72	0.04
NCM 7050	1 k, 2 FET cell	160 x 154	2.72	0.11
NCM 7051	1 k, 2 FET cell	169 x 171	2.48	0.09

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Figure 1-8 shows the details of the memory cell. It is conventional in form and conservative in dimensioning. Separate source and drain diffusions are provided for each memory transistor. A cell requires one metal line and four diffused lines. No contact windows to silicon exist. Four masks are used to form the cell, and alignment is not critical. All features are stripes compatible with present day 4-micron technology.

In MNOS cell designs a limiting factor has been the dimensional pitch achievable by the circuitry on the periphery of the array. For example, the pitch of the word address circuitry (row decoder) in the 6000C device determined the vertical dimensions of the array. In the 6002 approximately the same decoder pitch was maintained, but two decoders were used. By bringing the row selection circuits into both sides of the array to interleaved rows, the cell density was almost doubled.

Examination of the die photo shows little wasted space in the peripheral circuit areas. The layout maintained a 0.26 array to die area ratio even

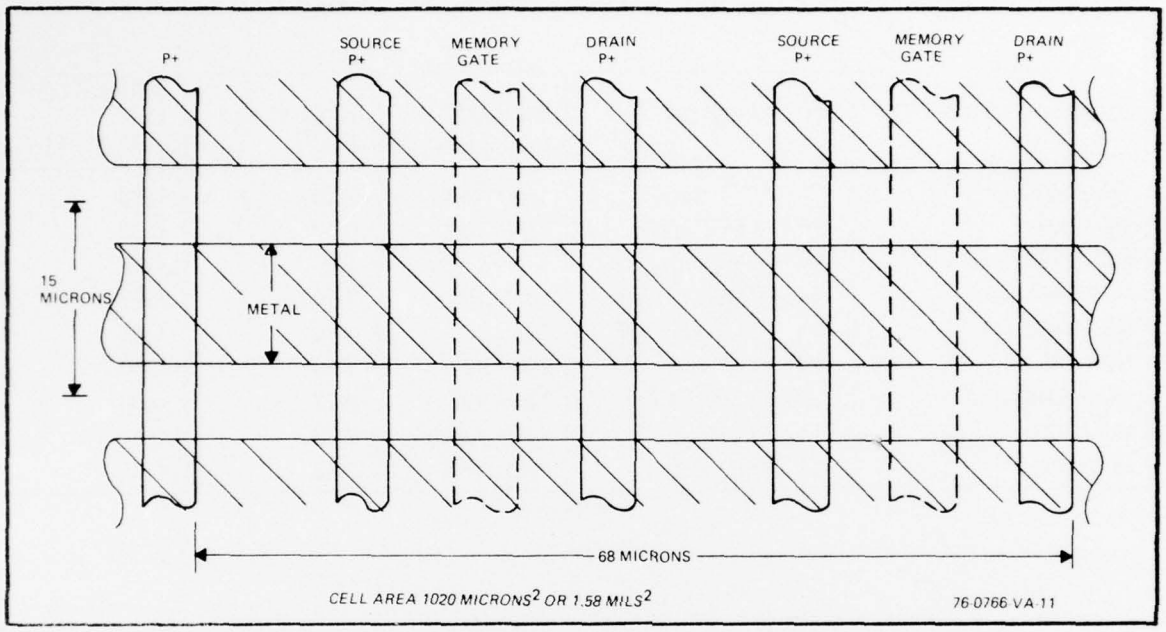

Figure 1-8. BORAM 6002 Two-Transistor Cell

with increased cell density. The 6002 die area is 46 percent of the 6000C area. The area reduction was achieved by approximately equal shrinkage of both array and peripheral circuitry.

As the functional block diagram of figure 1-7 shows, the 6002 contains a fully decoded 64-word by 32-bit RAM and a 32-bit dynamic two-phase shift register. All I/O takes place serially through the shift registers. Parallel bidirectional data transfer between the RAM and the shift register takes place via an internal 32-bit latch.

The RAM and shift register can operate independently. This allows the RAM to be writing data from the latch into the memory array while new data is being shifted into the register. High bit rates may be maintained at the I/O terminals while the RAM need operate at only 1/32 of the external rate. In a practical BORAM system working into standard military interfaces, maximum shift rates of a few hundred kilohertz will be required. Therefore,

write times on the order of 100 microseconds can be allowed without delaying the data flow.

It is an interesting aspect of the BORAM chip organization and the system application that no critical dynamic performance requirement is imposed on the chip. The chip performance capability greatly exceeds actual use conditions. For example, the shift registers operate quite well at 1 MHz, but are only required to operate at a few hundred kilohertz.

To store data in a memory cell, two operations are performed. First, the cell is cleared or initialized using the clear signal (CL). This places both memory transistors in the high condition threshold state. Second, the data present in the latch is written into the cell using the memory write ($\overline{MW}$) signal. In response to writing, one transistor in the cell is forced into the low conduction state, while the second transistor remains in the high conduction state.

The 6002 allows clearing of the entire chip with one pulse, or optionally allows clearing of 128 bits as a function of the address inputs and the control signal sequence. Writing takes place in 32-bit words as a function of the address inputs and the control signal sequence.

1.3.3 Initial Sample Analysis

During December, 10 wafers of BORAM 6002 chips cleared the production line. Device analysis was initiated, and two specific problems were identified. Detailed testing confirmed circuit operation. Confirmation of yield potential is expected during the first quarter of 1977.

Two problems were encountered with this first lot of material. A diffused cross under was found to be improperly located. Mask revisions are necessary to correct this error. Even with the cross under problem it was possible to operate the chip by making some timing adjustments to the control signals. Only the group clear mode of operation was impaired.

The second problem with the lot was low field inversion threshold voltage. Field inversion is controlled by an ion implant. The dose employed produced

a 28-volt threshold versus a desired 40-volt level. Implant conditions have been corrected for following lots.

The low field threshold prevented operation with the nominal chip select voltage of 35 volts. Writing and clearing times were increased to allow for operation at reduced voltages.

Detailed probe tests were performed to verify the operation of the chip circuitry at critical nodes. All functional blocks were found to be in reasonable agreement with computer simulation predictions.

Additional devices will be evaluated during the first quarter of 1977. Complete characterization test results and a device data sheet are expected to be available during the second quarter.

1.4 VT TESTER STATUS

The Westinghouse VT tester shown in figure 1-9 was developed to provide rapid feedback of MNOS transistor characteristics for line control purposes and reliability analysis. During this past quarter the final work to debug and verify the measurement circuitry was completed, and some initial measurements were attempted.

1.4.1 Equipment Description

Figure 1-10 shows the functional parts of the VT tester. The instrument measures the threshold voltage of one to eight transistors after application of programmed pulse sequences. As shown in figure 1-11, each test socket has a dedicated threshold detection circuit. The measured analog voltage is converted into a 12-bit binary word for storage in a data memory.

The VT tester can be used to perform 7 different types of tests. Table 1-3 shows how the operations are specified using 5 of the front panel switches. Table 1-4 shows how data is readout of the data memory using 2 other front panel switches.

For threshold decay measurements, the VT system applies preprogrammed signal sequences to the 8 devices to establish an initial condition. It then measures and stores the threshold voltage of each transistor at programmed read

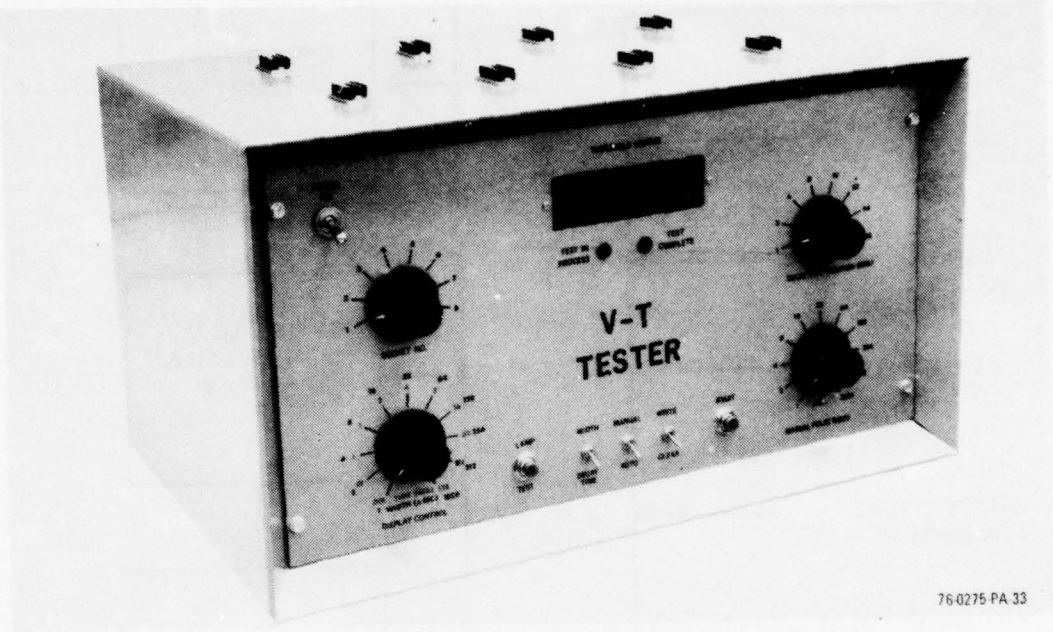

Figure 1-9. The Westinghouse VT Tester

delay times. Table 1-5 presents the test sequence for both clear and write threshold decay measurements. At the end of the test, the data stored in an internal memory can be readout on the front panel digital display. Preprogrammed read delay times begin at 0.001 hour (3.6 sec), and continue at intervals convenient for logarithmic plotting to a selectable maximum of 128 hours.

In a second operating mode, the VT tester will measure the threshold voltage as a function of the write (or clear) voltage pulsewidth. This is the so called "pulse response" characteristic of the memory transistor. Table 1-6 presents the pulse response test sequence for both the clear and write pulse response measurements.

At the beginning of a pulse response test, the VT system applies a sequence of signals to the 8 devices to establish a known initial condition. The devices are then appropriately pulsed, and the threshold after 3.6 seconds is read

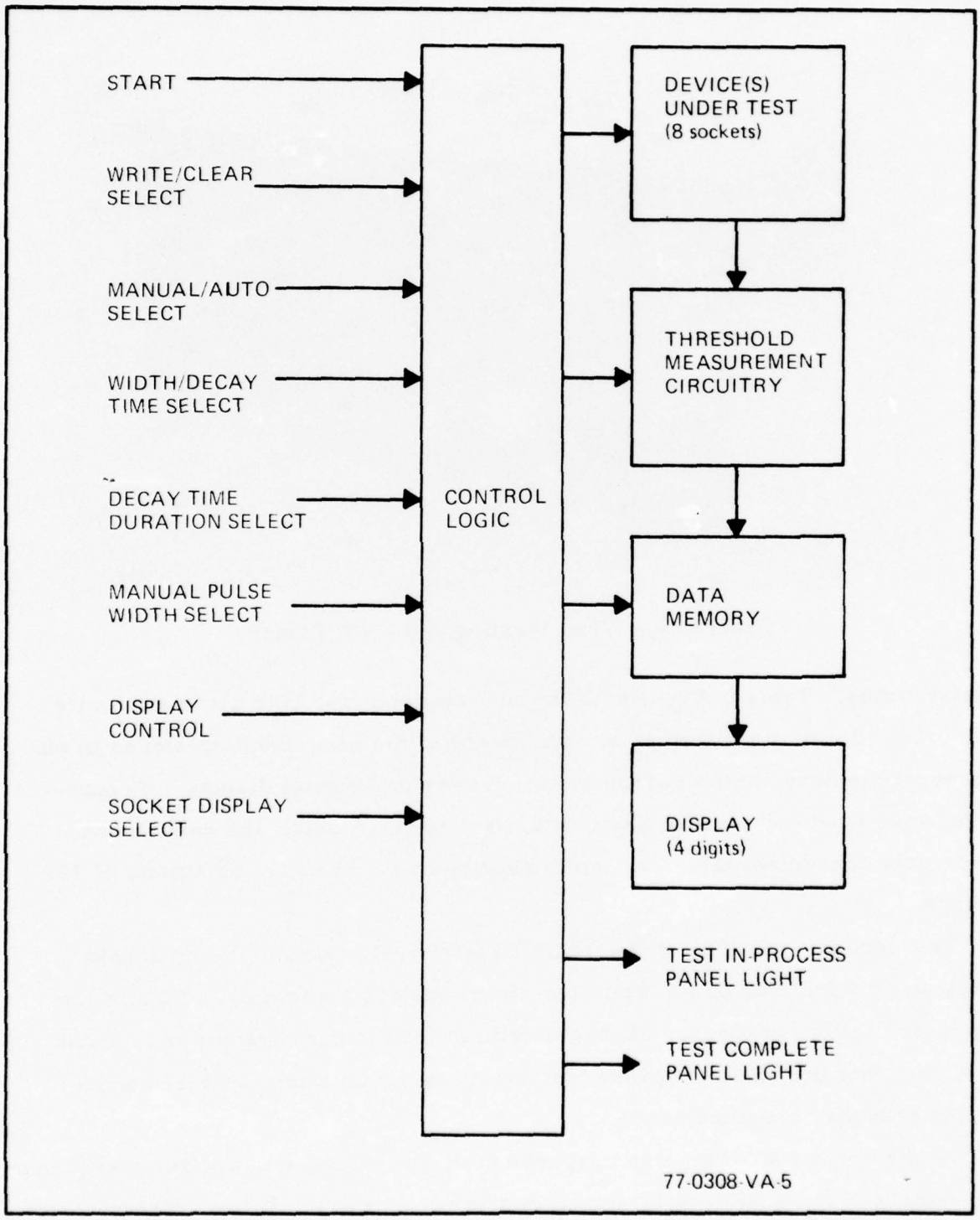

Figure 1-10. VT Tester Functional Block Diagram

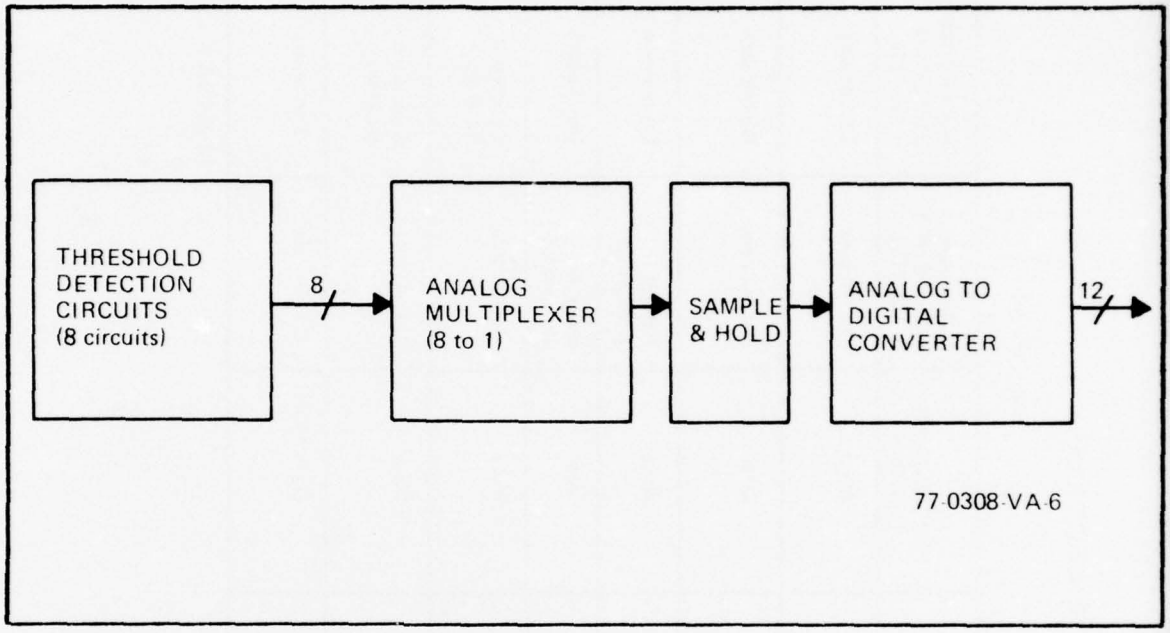

Figure 1-11. VT Tester Measurement Circuit Block Diagram

and stored. Pulsewidth is varied from 1 microsecond up to 1024 microseconds in a binary fashion (1, 2, 4...). At the end of the tests, the data accumulated in an internal memory can be readout on the front panel display.

1.4.2 Precision and Accuracy

Several experiments were conducted to examine the precision and accuracy of the VT tester. The design objective for the system was to maintain sufficient repeatibility so as to not distort threshold decay trend data or pulse response curves. Random variability in test results should not be large enough to noticably affect graphical displays. High accuracy is not essential. Performance comparable to curve tracer results is acceptable.

Table 1-7 presents some 96 threshold voltage measurements performed on three nonmemory transistors. The observations were taken on 4 different days in each of 8 test sockets. Based on this data, it is reasonable to expect that more than 99 percent of the time a given measurement can be repeated within ±30 mV or about ±1 percent.

TABLE 1-3

VT TESTER OPERATION SELECTION

SELECTED TEST PROGRAM	WIDTH/DECAY TIME SWITCH	MANUAL/AUTO SWITCH	WRITE/CLEAR SWITCH	MANUAL PULSEWIDTH SWITCH	DECAY TIME DURATION SWITCH
Write pulse response Automatic scan from 1 to 1024 μsec widths	Width	Auto	Write	Do not care	Do not care
Clear pulse response automatic scan from 1 to 1024 μsec widths	Width	Auto	Clear	Do not care	Do not care
Write pulse response single selected pulsewidth	Width	Manual	Write	Selects pulsewidth	Do not care
Clear pulse response single selected pulsewidth	Width	Manual	Clear	Selects pulsewidth	Do not care
Write threshold decay automatic delayed read at programmed intervals	Decay time	Auto	Write	Do not care	Selects test duration
Clear threshold decay automatic delayed read at programmed intervals	Decay time	Auto	Clear	Do not care	Selects test duration
Threshold measurement write/clear pulses are suppressed	Decay time	Manual	Do not care	Do not care	Do not care

77-0308-VA-7

TABLE 1-4

VT TESTER READ-OUT SELECTION

FRONT PANEL CONTROL SWITCH	DESCRIPTION OF CONTROL SWITCH FUNCTION
SOCKET NUMBER	Data memory is partitioned into 8 sections. Each section contains data associated with a given test socket. The "SOCKET NO." switch selects which of the 8 data sets is routed to the display.
DISPLAY CONTROL (Does not affect the display if manual/auto switch is in manual position)	The "DISPLAY CONTROL" switch selects which data word within a section of memory is to be displayed. The labels on the switch identify the significance of the displayed threshold voltage. For pulse response tests the switch setting indicates the pulsewidth. For threshold decay tests the switch setting indicates the read delay time.

77-0308-VA-8

TABLE 1-5

VT TESTER THRESHOLD DECAY TEST SEQUENCES

TYPE TEST	TEST PROGRAM SEGMENT	ELECTRICAL TEST CONDITIONS
CLEAR THRESHOLD DECAY	Precondition Sequence (repeated 16 times)	1. Write VGS = –24V, 3.6 sec 2. Clear VGS = +20V, 1024 μsec
	Decay Time Test Sequence (maximum read delay time is selected by the DECAY TIME DURATION switch)	Read VHC threshold at 10 μA for read delay times of 0.001 hr, 0.01 hr, 0.1 hr, 1 hr, 2 hr, 4 hr, 8 hr, 16 hr, 32 hr, 64 hr, and 128 hr.
WRITE THRESHOLD DECAY	Precondition Sequence (repeated 16 times)	1. Clear VGS = +20V, 3.6 sec 2. Write VGS = –24V, 128 μsec
	Decay Time Test Sequence (maximum read delay time is selected by the DECAY TIME DURATION switch)	Read VHC threshold at 10 μA for read delay times of 0.001 hr, 0.01 hr, 0.1 hr, 1 hr, 2 hr, 4 hr, 8 hr, 16 hr, 32 hr, 64 hr, and 128 hr.

77-0308-VA-9

TABLE 1-6

VT TESTER PULSE RESPONSE TEST SEQUENCES

TYPE TEST	TEST PROGRAM SEGMENT	ELECTRICAL TEST CONDITIONS
CLEAR PULSE RESPONSE	Precondition Sequence (repeated 15 times)	1. Write VGS = −24V, 3.6 sec 2. Clear VGS = +20V, 1024 μsec
	Response Test Sequence Auto Mode: Scanned for 11 values of n (1, 2, 4, 8 ... 512, 1024). Manual Mode: Only 1 value of n selected by MANUAL PULSEWIDTH switch.	1. Write VGS = −24V, 3.6 sec 2. Clear VGS = +20V, n μsec 3. Delay 3.6 sec 4. Read VHC threshold at 10 μA
WRITE PULSE RESPONSE	Precondition Sequence (repeated 15 times)	1. Clear VGS = +20V, 3.6 sec 2. Write VGS = −24V, 128 μsec
	Response Test Sequence Auto Mode: Scanned for 11 values of n (1, 2, 4, 8 ... 512, 1024). Manual Mode: Only 1 value of n selected by MANUAL PULSEWIDTH switch.	1. Clear VGS = +20V, 3.6 sec 2. Write VGS = −24V, n μsec 3. Delay 3.6 sec 4. Read VLC threshold at 10 μA

77-0308-VA-10

TABLE 1-7

VT TESTER NONMEMORY TRANSISTOR THRESHOLD MEASUREMENTS

Nonmemory Transistor Sample	Date of Test	Threshold Voltage Measured in Each Test Socket (Volts)							
		1	2	3	4	5	6	7	8
1	14 Dec	2.845	2.840	2.840	2.835	2.845	2.840	2.850	2.845
	16 Dec	2.880	2.870	2.870	2.875	2.880	2.880	2.885	2.875
	20 Dec	2.865	2.850	2.860	2.855	2.855	2.860	2.875	2.860
	6 Jan	2.865	2.845	2.850	2.850	2.850	2.855	2.860	2.850
2	14 Dec	2.925	2.935	2.930	2.925	2.935	2.925	2.925	2.930
	16 Dec	2.920	2.910	2.915	2.910	2.935	2.920	2.930	2.920
	20 Dec	2.920	2.925	2.920	2.915	2.925	2.920	2.930	2.920
	6 Jan	2.925	2.920	2.920	2.920	2.940	2.925	2.930	2.925
3	14 Dec	2.965	2.965	2.965	2.960	2.975	2.970	2.970	2.965
	16 Dec	2.955	2.950	2.955	2.955	2.970	2.960	2.965	2.955
	20 Dec	2.960	2.955	2.960	2.955	2.965	2.960	2.965	2.955
	6 Jan	2.960	2.955	2.960	2.955	2.975	2.965	2.975	2.955

77-0308-VA-11

Sample	Variance
1	1.960,000E-4
2	0.491,401E-4
3	0.461,041E-4
Average	0.970,814E-4

From the average variance, a standard deviation of 9.853 mV is obtained. Therefore, the three standard deviation range is ±29.558 mV or 1.014 percent of the mean. Sample 1 was the major contributor to the variance. This device exhibited a shift in threshold with the date of the observation. This implies that the data reflects a real shift in characteristics of this particular device (the other two samples do not show such changes), and therefore, the prediction of precision for the instrument is pesimistic.

To gain some idea of the accuracy of VT tester threshold measurements comparisons were made with data obtained by other means. A digital voltmeter and variable voltage sources were used in the laboratory to measure the gate to source voltage for a drain current of 10 microamperes. The arrangement allowed resolution of the threshold voltage to 10 millivolts. Table 1-8 compares 25 VT tester measurements to data obtained by the lab equipment.

The mean difference was 39 millivolts. The standard deviation was 22.64 millivolts. The standard deviation of the mean was 4.53 mV. Assuming normal distributions, 99 percent of the time the two measurements will agree within a range of 27 to 50 millivolts.

The VT tester is expected to provide better than 2 percent accuracy at its present state of development. In the future the circuitry will be further refined to reflect actual test experience. Differences between test sockets can be corrected by bias adjustments. Some experimental work needs to be done on possible drift of the threshold readings with temperature.

1.4.3 Sample Test Results

To illustrate the nature of the data obtained from the VT tester, a few parts have been tested and the results were plotted.

TABLE 1-8

COMPARISON OF VT TESTER AND LABORATORY INSTRUMENTED THRESHOLD MEASUREMENTS

Sample Number	Threshold Voltage at 10 μA		Difference
	VT Tester*	Laboratory Equipment	
	Volts	Volts	Millivolts
1	3.125	3.08	45
2	3.230	3.19	40
3	3.160	3.11	50
4	3.200	3.16	40
5	8.120	8.01	110
6	4.280	4.22	60
7	3.495	3.44	55
8	3.930	3.86	70
9	3.440	3.42	20
10	3.385	3.35	35
11	3.420	3.40	20
12	3.435	3.41	25
13	4.315	4.26	55
14	3.465	3.46	5
15	3.295	3.27	25
16	3.050	2.99	60
17	3.290	3.27	20
18	3.305	3.26	45
19	3.105	3.08	25
20	3.000	2.98	20
21	3.235	3.22	15
22	2.625	2.61	15
23	3.255	3.23	25
24	3.560	3.51	50
25	3.455	3.41	45

*Measured in test socket 1.

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Table 1-9 presents the threhold decay results from 3 sample devices. The devices were chosen because of widely different decay rates. A regression analysis was performed, and all parts were found to have a linear decay with the logarithm of read delay time. The slope, intercept and correlation coefficient appear at the bottom of the table. The results are presented graphically in figure 1-12.

Table 1-10 presents write pulse response results for 3 sample devices. Figure 1-13 provides a graphical view of the data. Between the 1 and 2 microsecond widths the transistors fail to respond, and the curves flaten out.

1.5 AUGER AND SPUTTERING ANALYSIS RESULTS

A series of experiments have been run to evaluate the tunneling layer and nitride film. Auger microprobe facilities located at the Westinghouse Research Laboratory in Pittsburgh were employed.

1.5.1 Description of the Auger Equipment

The PHI-SAM microprobe manufactured by Physical Electronics Industries was employed for this phase of the study. It is a scanning type probe which can perform analyses on spots as small as 6 micrometers in diameter. Auger electrons are excited by a primary electron beam. The energy of these Auger electrons is determined by a cylindrical mirror type charged particle energy separator. Using this separator, an Auger electron of energy E can be viewed as distinct from an Auger electron of energy E as long as the inequality:

$$\frac{|E - E'|}{E} = \frac{\Delta E}{E} \geq 0.006$$

is satisfied. In other words, the energy resolution of the electron spectrometer is 0.6 percent. In order to view low level signals above noise, the derivative of the Auger spectrometer signal (usually called the dN(E)/dE spectrum) is displayed, rather than the time signal.

TABLE 1-9

THRESHOLD DECAY MEASUREMENTS

Decay Time t_{rd} Hours	Threshold Voltage V_T at 10 μA (Volts)		
	Sample 2838A-1	Sample 2838A-2	Sample 2838A-3
0.001	6.860	10.075	7.510
0.01	6.585	9.310	7.060
0.1	6.330	8.520	6.620
1.0	6.075	7.705	6.195
2.0	6.005	7.465	6.075
4.0	5.930	7.215	5.935
8.0	5.860	6.985	5.815
16.0	5.790	6.740	5.690
32.0	5.715	6.500	5.560
Intercept (Volts)	6.086	7.702	6.202
Slope $\left(\frac{\text{Volts}}{\text{Decade}}\right)$	−0.253	−0.797	−0.431
Correlation Coefficient	0.99971	0.99995	0.99991

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The equipment features an ultra-high vacuum chamber. Typical base pressures of 10^{-10} T are achieved using oil free pumps. The ultimate design pressure is 5×10^{-11} T as measured by an N_2 equivalent pressure guage.

Sputtering is performed on the samples analyzed using an argon ion beam. These argon ions are accelerated to an energy of 20 KeV, providing a beam current density of 180 $\mu A/cm^2$. Typical sample sputtering rates with this beam vary from 10 to 240 Å/min. For analysis with a primary ion beam energy less than 3 KeV, a grazing incidence electrons gun is available.

Auger electron spectroscopy (AES) is useful in determining chemical compositions of volumes of surface material whose depth varies from 3 to 20 Å beneath the sample-vacuum interface. The depth of analysis depends on the escape distance of the Auger electron. This distance is a function of the sample composition and the energy of the Auger electron. Selection

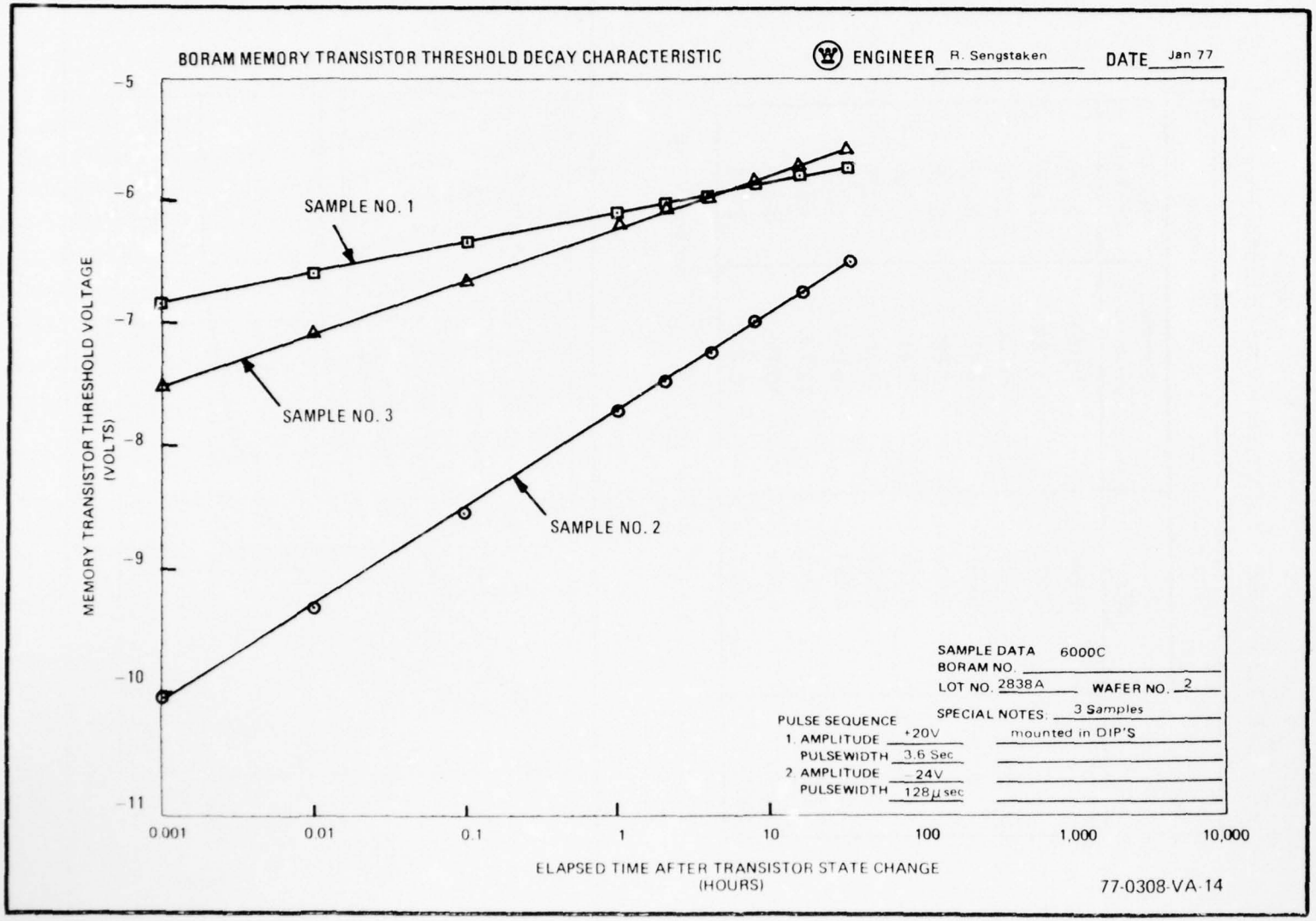

Figure 1-12. Threshold Decay Curves for 3 Sample Transistors

TABLE 1-10

WRITE PULSE RESPONSE MEASUREMENTS

Write Pulse-width μsec	Threshold Voltage VT at 10 μA (Volts)		
	Sample 2838A-1	Sample 2838A-2	Sample 2838A-3
1	2.995	2.830	2.820
2	3.075	4.185	2.855
4	4.115	6.830	5.095
8	5.060	8.125	6.205
16	5.695	8.885	6.755
32	6.205	9.415	7.100
64	6.595	9.785	7.335
128	6.850	10.015	7.485
256	6.975	10.130	7.525
512	6.995	10.155	7.495
1024	6.990	10.155	7.465

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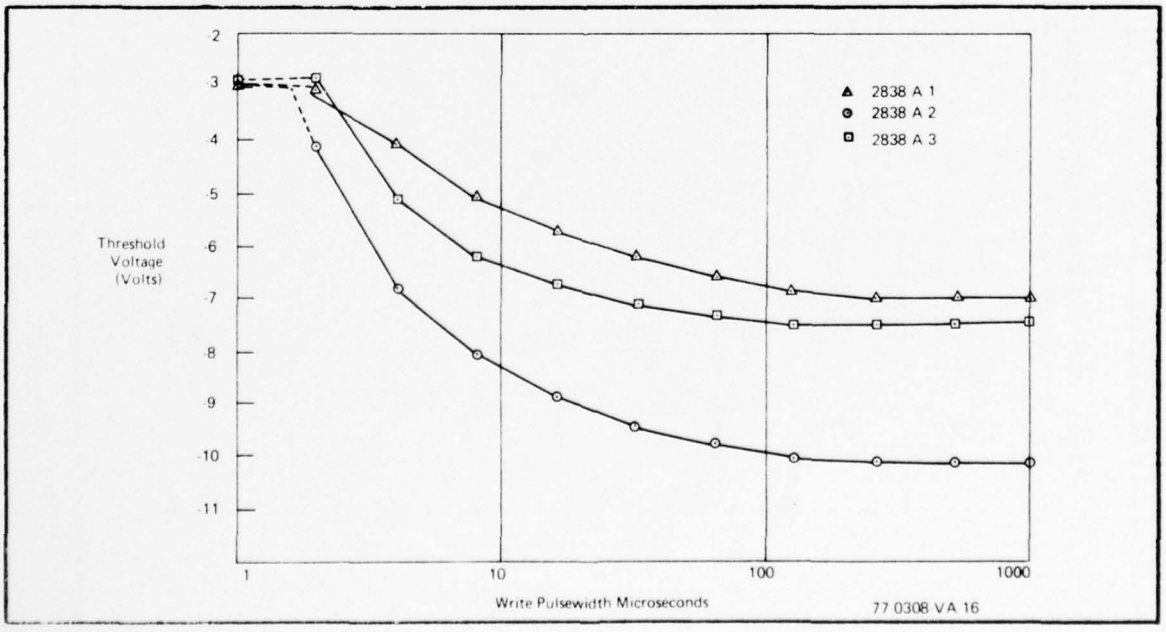

Figure 1-13. Write Pulse Response Measurements

limits for different atomic species range from 0.1 to 0.02 atomic percent. In some cases, information concerning the valence state of the species analyzed can be obtained.

1.5.2 Tunnel Layer Analysis

Five thin oxide samples of two wafers each were prepared for Auger analysis. The material was N type (100) silicon with 4 to 8 ohm centimeter resistivity. The five samples differed in surface treatment.

a. HF strip, no cleaning
b. HF strip, prenitride clean
c. HF strip, prenitride clean, HCl treatment
d. HF strip, prenitride clean, HCl treatment, N_2 treatment
e. HF strip, prenitride clean, N_2 treatment

To the limits of experimental accuracy no differences could be found between samples a, b and c. An oxide film was detected, and metallic silicon was observed. This latter fact indicates either an oxide film <14 Å or the presence of unbonded silicon in the oxide. Carbon was observed in trace quantities ($\approx$1 atomic %) in all films.

Thickness for these samples was estimated using the sputtering rate of stoichiometric silicon dioxide as a guage. The layers were approximately 3 monolayers (≈ 11 Å).

No chlorine was detected in the HCl treated film. This places an upper bound on chlorine incorporation at the Auger detection threshold of 0.1 atomic percent.

Samples d and e had thicker surface films. Sample d was estimated at 5 monolayers (≈ 18 Å). Sample e had more than 11 monolayers (≈ 39 Å).

The chemical composition of samples d and e differed from the previous samples in that nitrogen was present. Sample d showed about 1 atomic percent. The first wafer of sample e contained about 4 atomic percent, and the second wafer contained about 20 atomic percent.

These experimental findings are significant in the context of normal processing. During the nitride reactor predeposition cycle the tunneling layer is exposed to nitrogen. Non-HCl treated films tend to incorporate nitrogen in variable amounts. This affects reproducibility and pulse response.

1.5.3 Nitride Film Analysis

Experiments have been performed on nitride films, but the results are unclear because of nitride reactor equipment problems.

Four samples were prepared for analysis. Samples a, b, and c consisted of nitride deposited on HCl treated tunneling layers. The d sample was fabricated without HCl treatment.

Capacitors formed on samples a and b were found to be electrical defective. Samples c and d showed normal electrical performance.

Auger analysis indicates 1 to 5 atomic percent of carbon and oxygen contamination for samples a and b. This was believed to originate from the nitrogen supply to the nitride reactor. (This problem has since been eliminated.)

Samples d and e were identical in chemical composition under Auger analysis. Film stoichiometry was constant through the films to within 50 Å of the silicon surface. Trace oxygen was detected at less than 1 atomic percent. Trace carbon was also detected at less than 1 atomic percent.

1.6 PRODUCTION ACTIVITY

During the second quarter of the MM&T project production effort matured considerably. Engineering sample fabrication was well underway, and yields rose above objectives.

1.6.1 Engineering Sample Fabrication

Fabrication was seriously delayed during the first quarter of activity by nitride reactor problems. Considerable amounts of material were placed on hold at in-line stations before nitride deposition. At the end of September 1976, the cumulative wafers tested were 29 against a plan of 78.

Table 1-11 shows the status as of the end of December. The 64 percent deficit of wafers tested in September has been reduced to an 8 percent deficit in December. Sufficient chips have been produced to meet engineering sample deliveries, and an inventory for test purposes will soon be accumulated. Table 1-12 presents the plan for 6000C production during January.

Table 1-13 shows the process line inventory status as of the end of December. The target inventory level for process tuning is approximately 100 wafers spread evenly across all line operations.

1.6.2 Production Plan for Next Period

The production of 6000C die will continue during the next quarter to provide chips for engineering sample assembly and for process experimentation. The 6000C will be used as the vehicle for confirmation of 3-inch wafer production. Some 2-inch wafer production will continue through the period.

Prototype runs of 6002 die will be evaluated, and the mask set will be modified to correct any problems. After design verification is complete,

TABLE 1-11

ENGINEERING SAMPLE FABRICATION STATUS

Event	Status to 31 December 76		
	Plan	Actual	Deviation
Wafer Starts	360	402	42
Wafer Completions	195	179	(16)
Wafers Tested	195	166	(22)
Chips Complete	694	347	(347)

77-0308-TA-17

TABLE 1-12

JANUARY PRODUCTION PLAN

Event	Cumulative Dec 1976 Status	Jan 1977 Plan	Expected Jan 1977 Status
Wafer Starts	402	100	502
Wafer Competitions	179	82	261
Wafers Tested	166	95	261
Chips Completed	347	285	632

77-0308-TA-18

TABLE 1-13

INVENTORY STATUS (12/31/76)

Station	Code	Quantity	% of Process Complete
Epi/Laser	120	10	0
N+ Photo	151	20	20
Phos Dep	160	0	25
Mem Photo	191	27	43
SiN Dep	200	26	50
Test	271	0	93

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runs will be made to characterize product variability. Conversion from 6000C to 6002 as the primary production vehicle is expected late in the quarter, or early in the following quarter.

1.6.3 Production Line Computer Model

The MM&T project requires achievement and verification of specific production rates. One tool to obtain visibility into individual station loading and through put is a computer model of the line.

Westinghouse has a computer program called "ORACLE" which is being modified to accommodate the BORAM production flow. Time values for 90 percent of the operations have been determined. Software modules containing station time value, loading factor, labor input, and other key variables are being compiled.

1.6.4 Nitride Etching Studies

Final nitride thickness differs from the deposited thickness because of some loss during oxide etch processing. The amount of nitride removed is depondent on the process used for nitride deposition.

Wafers obtained from two different nitride processes using the vertical rotary reactor were examined for thickness changes. Table 1-14 presents the results for the VRR/CDR process, and table 1-15 presents the results for the VRR/VDR process.

1.6.5 Vertical Rotary Reactor

A program has been initiated to improve the uniformity of the nitride films obtained from the AMV1200 vertical rotary reactor. Three recent unformity experiments show coefficients of variation ranging from 7 to 9 percent within 21 wafer runs.

1.6.6 LPCVD Nitride Films

Nitride deposition using low pressure chemical vapor deposition (LPCVD) systems is being evaluated. Superior thickness control and uniformity has been demonstrated previously. Figure 1-14 presents pulse response data achieved using four alternative tunnel layer processes and LPCVD nitride. The measurements were performed on capacitor structures.

TABLE 1-14

VRR/CDR NITRIDE ETCH LOSS

Wafer Number	Nitride Film Thickness (Angstroms)		
	Deposited	After Etching	Difference
1	460	415	45
2	535	485	50
3	565	535	30
4	515	480	35
5	575	515	60
6	540	480	60
7	635	595	40
8	500	465	35
9	475	430	45
10	475	435	40
11	565	540	25
12	525	495	30
Mean	530	489	41
Standard Deviation	52	51	11

77-0308-TA-19

TABLE 1-15

VRR/VDR NITRIDE ETCH LOSS

Wafer Number	Nitride Film Thickness (Angstroms)		
	Deposited	After Etching	Difference
1	455	405	50
2	455	415	40
3	506	445	61
4	480	415	65
5	370	330	40
6	548	485	63
7	498	445	53
8	551	475	76
9	475	385	90
10	410	365	45
Mean	475	417	58
Standard Deviation	56	48	16

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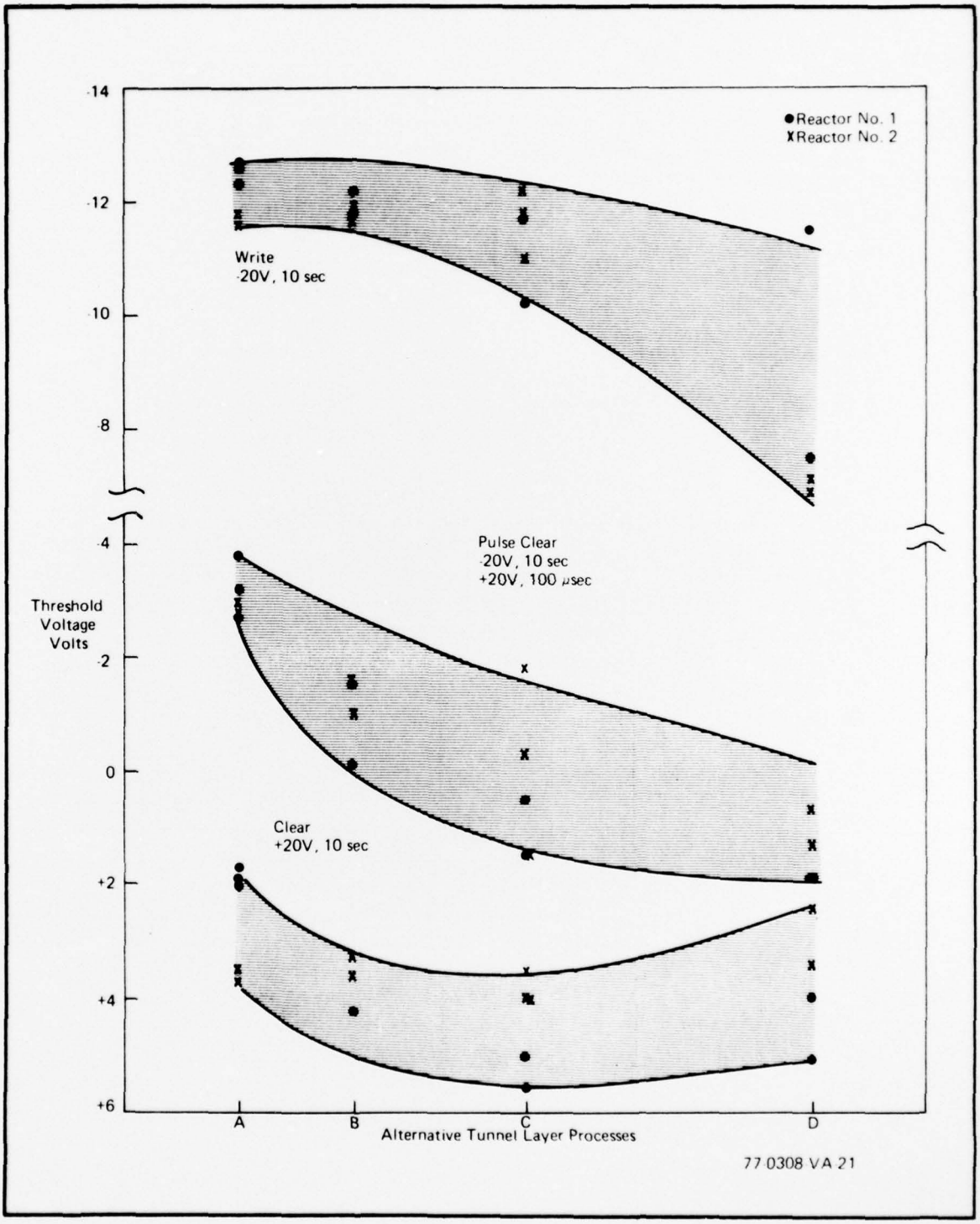

Figure 1-14. LPCVD Nitride Pulse Response

2. CONCLUSIONS

The second quarter of effort on the BORAM manufacturing methods project has been a period of steady achievement. The three week schedule delay encountered during the first quarter has lengthened to four weeks, but progress has been made on major problem areas.

Additional data on process variability has been obtained. The VT tester is now available to help gather data on pulse response and threshold decay. Test programs for probe test and hybrid circuit test are maturing.

The initial experience with the new low cost BORAM 6002 integrated circuit has been very promising. While much more work remains, the 6002 has been verified to function properly. The reduced cost of this chip greatly enhanced the probability of success of the manufacturing methods project, and of BORAM systems applications.

3. PROGRAM FOR NEXT INTERVAL

The immediate focus of the manufacturing methods project will be on the preparation and delivery of the first set of engineering samples within the month of January. The samples consist of 17 multichip hybrids and contain a total of 272 BORAM 6000C chips.

Several significant events are expected during the next interval. The BORAM 3-inch wafer line will begin operation. Hybrid circuit substrate design will be completed. Memory card design will be initiated. The first packages for the hybrids should be received.

Progress on the manufacturing methods project has direct impact on what can be achieved in the fabrication of BORAM storage systems. During the month of February, it is planned to invite government personnel to the Defense and Electronic Systems Center for a briefing on BORAM status and potential.

4. PUBLICATIONS AND REPORTS

During the past quarter, there were no publications or reports derived directly from this MM&T project.

5. IDENTIFICATION OF TECHNICIANS

The following key engineers and management personnel were employed on the BORAM manufacturing methods project during October, November and December of 1976.

Technician	Manhours
J. Brewer	248
M. Peckerar	168
C. Waldvogel	48
T. O'Donnell	89
P. Smith	363
L. Epstein	105

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